

FIG. 1

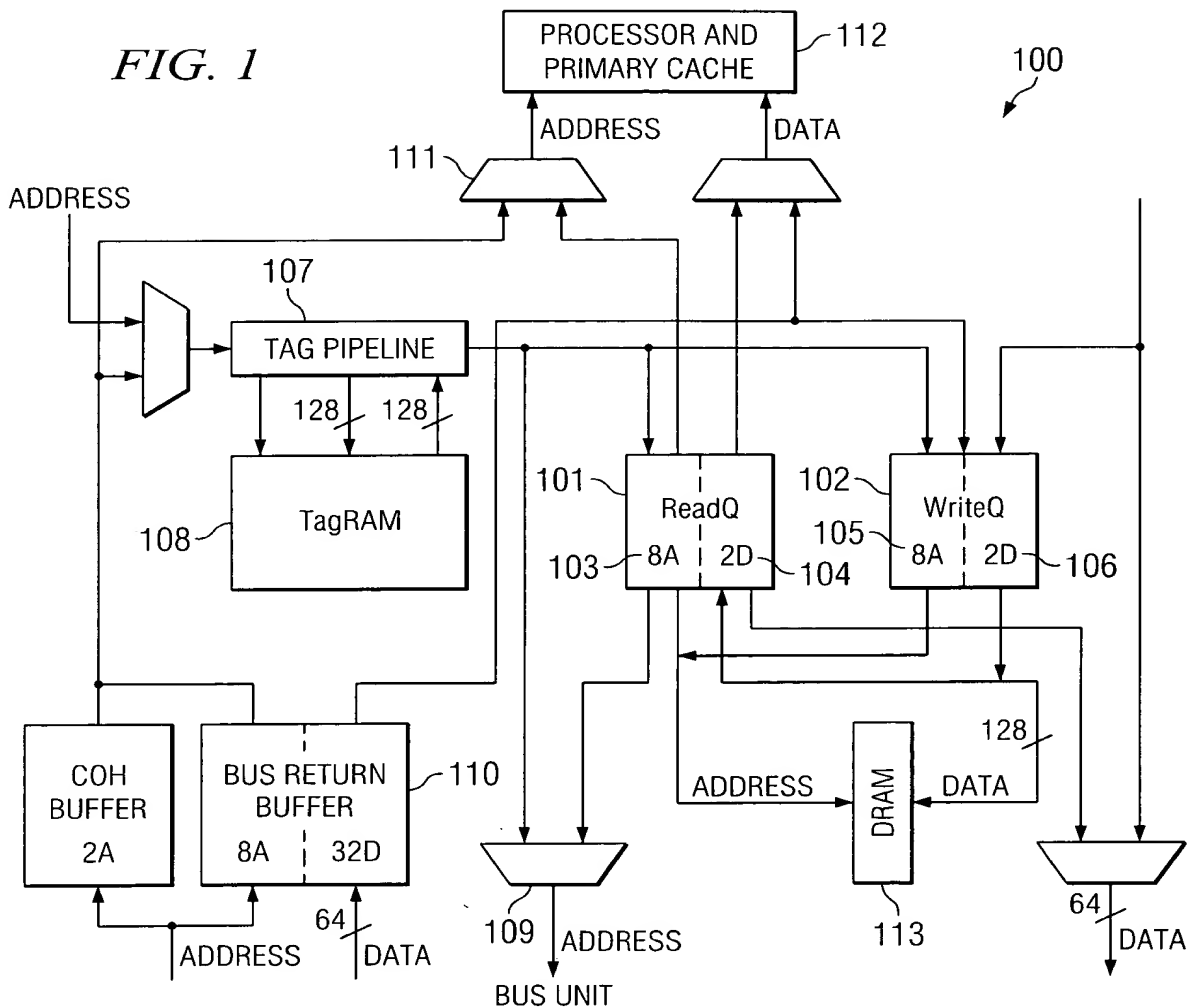
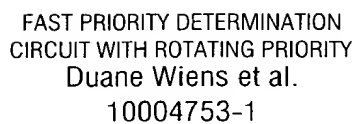


FIG. 2

		WAYS			
		0	1	2	3
INDICES	00000000000000001				
	00000000000000010				
	⋮				
	11111111111111111				

201





500
↙

FIG. 5

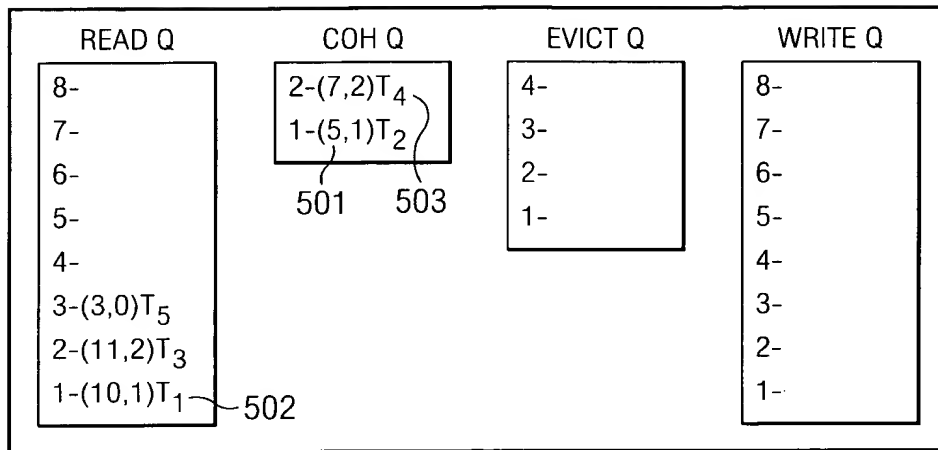


FIG. 6

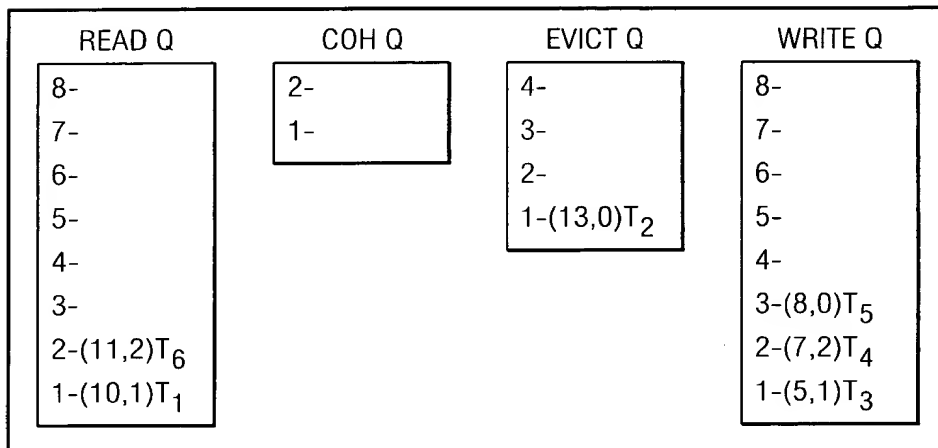


FIG. 7A

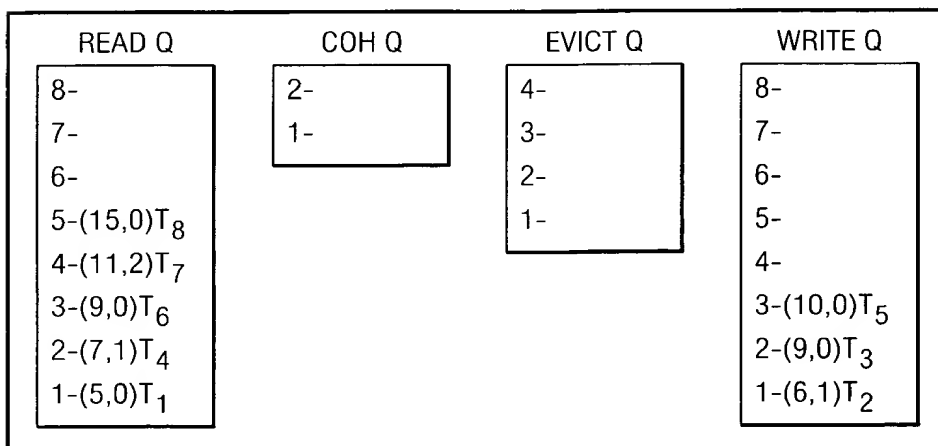




FIG. 7B

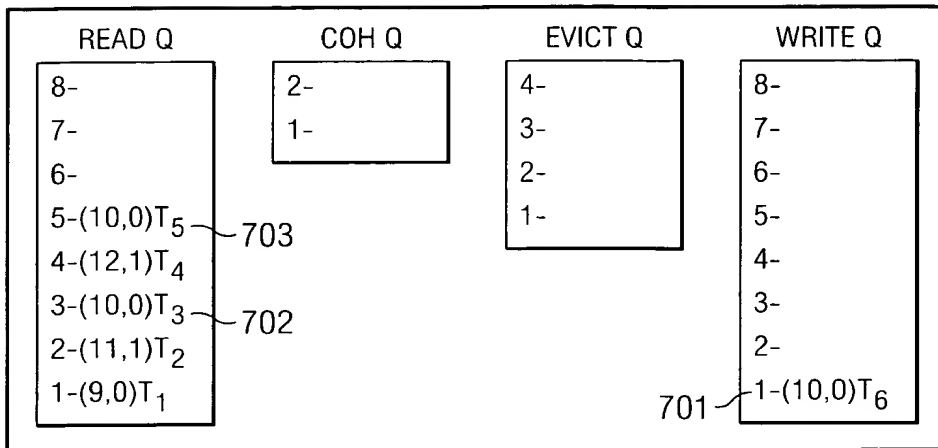


FIG. 7C

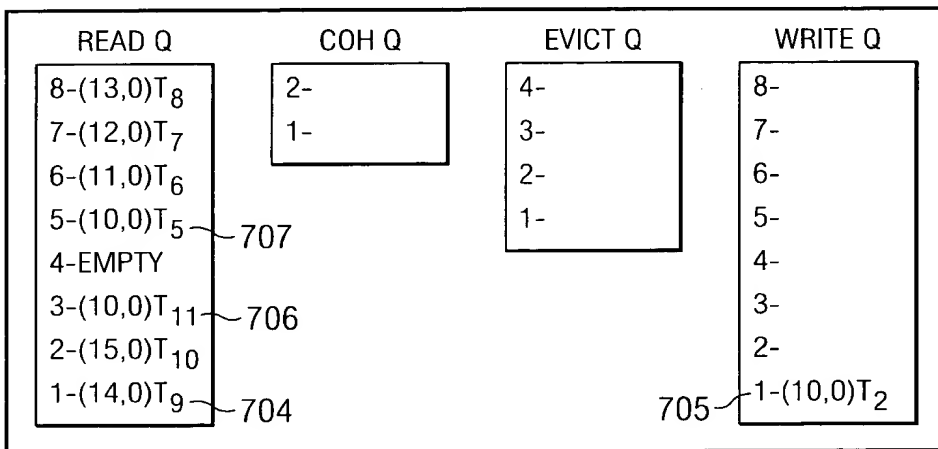


FIG. 9

		901	
900	ORIGINAL MATCH BITS	0001	0100
COUNTER VALUE=3			
902	RIGHT SHIFTED BITS	1000	0010
903	CLEAR MASK	0111	1111
904	APPLIED MASK	1000	0000
	REVERSE SHIFT	0000	0100

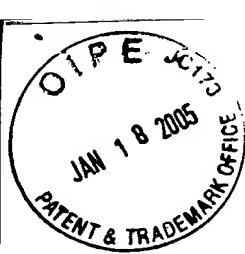


FIG. 8

800

801

802

SECOND (NEXT)

FIRST (PENDING)

TRANSACTIONS ON A SINGLE DRAM ADDRESS	READ Q	COH Q	EVICT Q	WRITE Q
↓	↓			
READ Q	IN ORDER 803	DC 808	DC 807	DEPENDENCY ENSURES READ FIRST, WRITE SECOND 814
COH Q	DC 812	IN ORDER 804	DC 809	HANDLED BY PRIORITY 816
EVICT Q	DC 811	DC 810	IN ORDER 805	EVICT FIRST WRITE SECOND DEPENDENCY 818
WRITE Q	WRITE FIRST READ SECOND DEPENDENCY 813	DEPENDENCY BETWEEN COH AND WRITE COH WAITS 815	WRITE FIRST EVICT SECOND DEPENDENCY 817	IN ORDER 806



FIG. 10

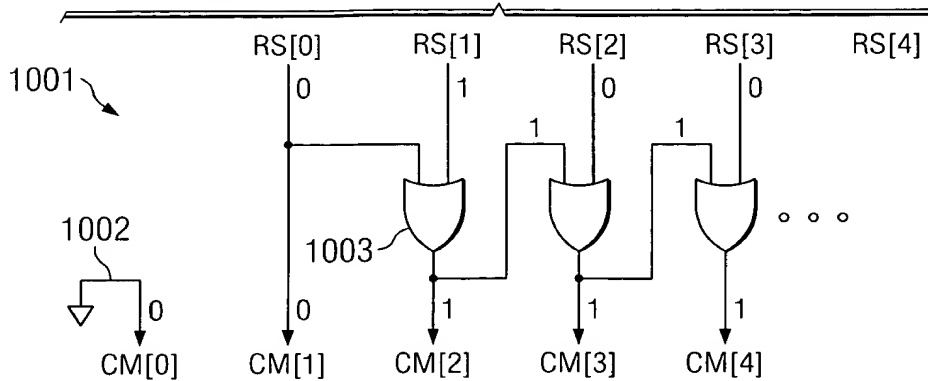


FIG. 11

900	ORIGINAL MATCH BITS	0001	0100			1100
	COUNTER VALUE = 3					
1101	DUPLICATE MATCH BITS	0001	0100	0001	0100	
1102	COUNTER MASK	0000	1111	1111	0000	
1103	MASKED MATCH BITS	0000	0100	0001	0000	
1104	CLEAR MASK	0000	0011	1111	XXXX	
1105	APPLIED MASK	0000	0100	0000	0000	
	ANSWER	0000	0100			

FIG. 12

